IN THE CLAIMS

Please amend claims as follows:

1. (Original) A semiconductor device with an OTP ROM formed over a semiconductor substrate including a memory cell area and a peripheral circuit area, the semiconductor device comprising:

a MOS transistor having a floating gate electrode, the MOS transistor being disposed at the memory cell area;

an OTP ROM capacitor having a lower electrode, an upper intermetal dielectric, and an upper electrode which are stacked in the order named, the OTP ROM capacitor being disposed over the MOS transistor; and

a floating gate plug connecting the floating gate electrode with the lower electrode,

wherein the floating gate electrode, the floating gate plug, and the lower electrode constitute a conductive structure which is electrically insulated.

2. (Original) The semiconductor device as set forth in claim 1, further comprising a capacitor that is disposed in the peripheral circuit area and includes a lower capacitor electrode, a dielectric film, and an upper capacitor electrode which are stacked in the order named.

3. (Original) The semiconductor device as set forth in claim 2, wherein the lower electrode and the upper electrode are identical to the lower capacitor electrode and the upper capacitor electrode in material and thickness.

4. (Original) The semiconductor device as set forth in claim 2, wherein the upper intermetal dielectric and the dielectric film are identical in material and thickness.

5. (Original) The semiconductor device as set forth in claim 1, wherein the upper intermetal dielectric is made of at least one selected from the group consisting of silicon oxide, silicon nitride and silicon oxynitride.

6. (Original) The semiconductor device as set forth in claim 1, wherein the upper intermetal dielectric is disposed over an entire surface of the semiconductor substrate.

7. (Original) The semiconductor device as set forth in claim 2, further comprising a lower intermetal dielectric formed below the upper intermetal dielectric.

8. (Original) The semiconductor device as set forth in claim 7, wherein the lower intermetal dielectric forms an OTP ROM opening and the upper electrode is formed in the OTP ROM opening.

9. (Currently amended) The semiconductor device as set forth in claim 2, wherein ~~the~~ a lower intermetal dielectric forms a capacitor opening and the upper capacitor is formed in the capacitor opening.

10. (Original) The semiconductor device as set forth in claim 1, further comprising a contact plug which is connected to an impurity region of the semiconductor substrate and is made of the same material as the floating gate plug.

11. (Original) The semiconductor device as set forth in claim 10, further comprising a bitline, the contact plug connecting the bitline to the impurity region of the semiconductor substrate.

12. (Original) The semiconductor device as set forth in claim 1, wherein the upper electrode comprises a first upper electrode and a second upper electrode disposed over the first upper electrode.

13. (Original) The semiconductor device as set forth in claim 2, wherein the upper capacitor electrode comprises a first upper capacitor electrode and a second upper capacitor electrode disposed over the first upper capacitor electrode.

14-29. Cancelled